FUNDAMENTALS OF SIGNAL INTEGRITY ANALYSIS

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ABSTRACT

New to Signal Integrity analysis, or just need to brush up on the fundamentals? If so, this white paper is for you.

The paper begins by identifying and analyzing critical nets in the design that may need signal integrity analysis. Next, it discusses transmission lines and the problems that arise from the high-frequency noise generated by rapid edge-rate signals. Finally, impedance is reviewed and discussed in the context of signal integrity.

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INTRODUCTION

Let's start this white paper on the fundamentals of signal integrity (SI) at the very beginning. Before you start doing any type of simulation or analysis, what do you have to do first, what information do you have to know? Your design probably has thousands of nets, will you simulate all of them? Probably not — there's not enough time for that and truthfully, it's not really necessary.

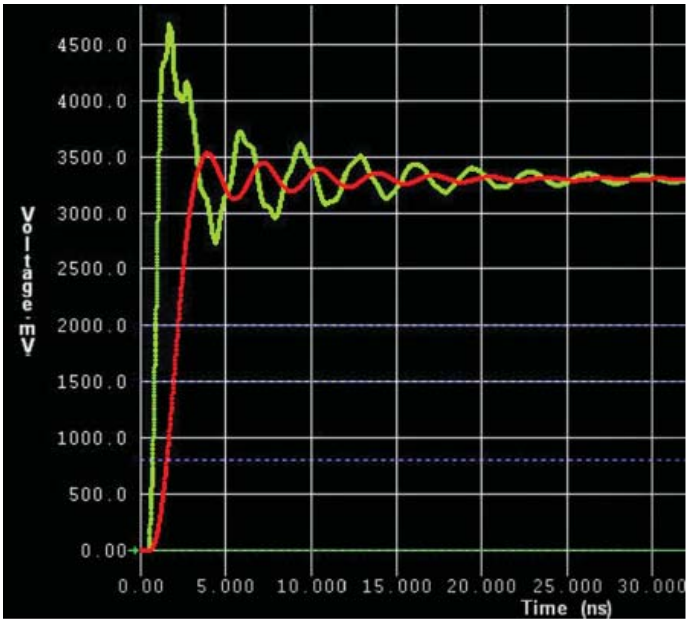
So, the first thing you have to do is determine what you care about — what are the "critical" nets in the design and what do you use to identify them?

CRITICAL NETS

At first glance, the answer to "what are the 'critical' nets?" may seem easy. I hear answers like "clock nets," "high frequency nets," "all the nets are critical," "nets faster than 100 MHz"…the list goes on and on. While these answers do have some merit, there is one defining characteristic of a net on a digital printed circuit board that you have to think about, and that's edge rate vs. trace length.

When you boil everything down and try to make a decision of which nets could cause you problems from an SI or electromagnetic interference (EMI) perspective, you want to look at the speed of the switching signal to determine if you care about that net first. As today's silicon processes scale deeper into the sub-micron space, the edge rates of signals become faster because of the physics of the device. That ultimately means that you have more potential problem nets on your design than you may have initially thought.

So we have some criteria for identifying a critical net, where do we find out this information to make the judgment call on what to analyze? The datasheet is the quickest place to check the characteristics of your device pins. You can find the voltage swing, the slew rate/switching time, input impedance, and a wealth of other information in these documents. But then you have to take that switching data and compare it to the trace lengths to find out if it's really a problem. It sounds complicated and possibly tedious (and if you had to do it by hand, it would be).



That's where you need to solicit the help of a tool. HyperLynx SI allows you to create simple models of your devices based on the datasheets and simulate nets to determine if there are problems based on those device characteristics and the traces. This is a first step, but an even more accurate step would be to use I/O Buffer models, better knows as IBIS models. IBIS models are a great source to determine the switching characteristics of your device. These are industry standard signal integrity models that most IC companies have available for www.mentor.com/pcb 1 designers so that you can successfully use their device in your design. HyperLynx SI can use this information to help you determine which nets to look at as well. It reads the IBIS information from the models and reports the length and copper delay of your nets, which allows you to quickly determine which nets you want to simulate.

If you were to do it by hand, it would take too much of your valuable time and be of minimal value, but with a quick scan from the results in HyperLynx SI, you know exactly where to look without a significant time investment.

You can do this first step — identifying critical nets — very early, before routing has started and you're doing your initial floor planning, or, you can do this in verification phase after routing is done. It's always best to start early though because that's going to give you the most benefit in the end, but the choice is yours.

TRANSMISSION LINES

Transmission line theory is the other half of the critical net equation. We're going to look at the mathematics, so you might want to break out your calculator!

Back in the "good ol' days," a transmission line carried your voice across the country – it's where we get the term landline. The point is that behavior across telephone lines is really not any different electrically than what is happening on your circuit board. If you ever made an international phone call before fiber-optic cable existed on the ocean floor, you can probably remember talking to someone, waiting a few moments and then the other person would hear what you said, you wait a little bit more and they respond.

It was slow and painful, but you knew that it took some time for your voice to travel halfway around the world. You didn't experience that when you called down the street or the next state over though, right? Intuitively, you knew that it took some time for your voice to travel a distance that far .

Now translate that to your circuit board. Because the distance between ICs on a PCB is relatively short (especially in comparison to a telephone line), people often don't think about the time it takes for signals to travel on the PCB. But time is relative, and for something that is switching with edge rates that are below 1 ns, that short distance between the ICs can seem like it's a trip halfway around the world. The delay of that trip, known as the velocity of propagation, is fairly easy to calculate, especially on typical FR4 PCB material.

Let's take a look at the math for the velocity of propagation:

$$Vp = c/\sqrt{(\mu \times Er)}$$

Velocity of Electromagnetic Propagation

Here c is the speed of light, $\mu = 1$ because we have non-magnetic materials, and Er is the dielectric constant. Typically for FR4, the dielectric constant is ~4.2. There is some variability to that number, but I won't get into that detail here. Going with that, we can see that Vp on a PCB is about equal to $Vp=c/\sqrt{4}$, which is about 1/2 the speed of light. That was easy math!

So we know that signals can travel about 6 inches per 1 ns from this quick and dirty math or invert that and you get 165 ps/inch. Let's call this propagation delay the trace delay. These are important (and handy) numbers to remember, so you might want to jot them down somewhere.

Those are cold hard facts about your PCBs electrical behavior as signals travel along traces, but now we get into the subjective part, which is critical length. Critical length compares that trace delay we just calculated to the edge rate of your signal to determine if we might have quality issues with that signal.

Many times, you'll see the rule of 1/3rd rise time to do this comparison. While this is a good starting point, it may not be good enough to meet your quality requirements. You may actually want to be more conservative and use a

rule like 1/6th rise time to catch potential issues. Here's a simple example using a 15 ohm driver with 1 V swing and a 1 ns edge rate. The receiver is a high Z CMOS input, and the transmission is 50 ohms with varying delay of rise time.

It's easy to see from the plot that we still have a substantial 300 mV of overshoot with a 1/3rd rise time rule and we may have missed this problem if we used that less conservative number.

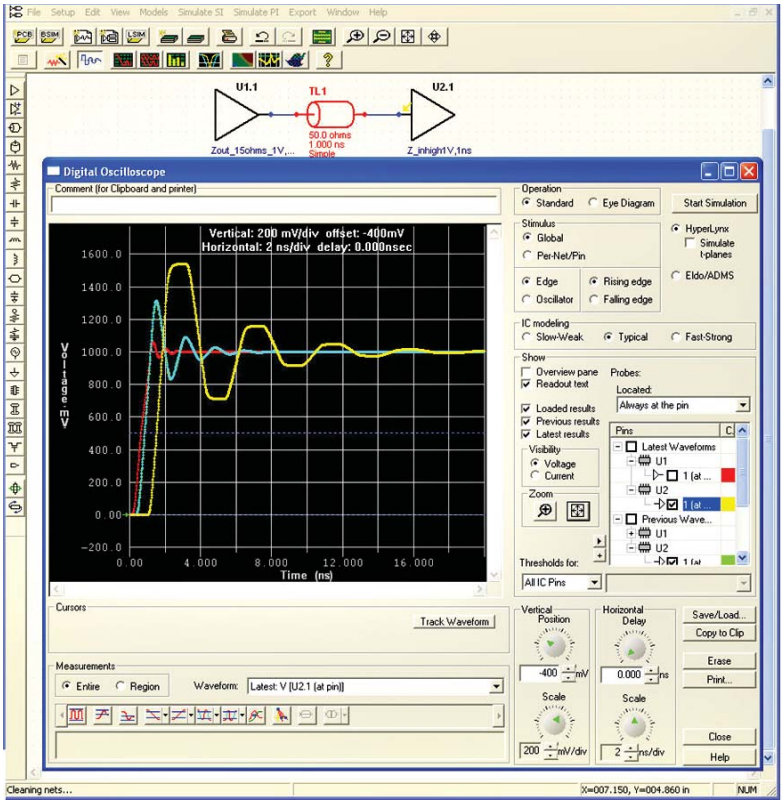
Regardless which fraction of your edge rate you choose, it's important to remember that the trace delay and the edge rate are closely tied to maintaining signal fidelity.

One thing I'll point out here is that I never talked about the operating frequency. The most important thing you can take away from this post is that signal quality depends on edge rate, not operating frequency. Look for those fast switching edges in your design, not just the buses that you think are fast because they have a 3Gbps differential pair.

IMPEDANCE

We're finally on to the last step in our study of signal integrity — impedance. So what is impedance and why does it matter?

Impedance is a result of the physical properties that make up your PCB and the reason you care about this is because the impedance of your traces will have an impact on the signal quality. If you remember from transmission lines, I talked about critical length. Well, one important aspect of transmission lines left out of that topic (on purpose) was that once transmission lines are beyond the critical length, the impedance becomes important because it can cause reflections and distort signal quality. Matching impedance for driver, transmission line, and receiver becomes important to ensure you have good signals at the receivers. Reflections are a topic in-and-of themselves, but below is what you need to know about transmission line impedance.



Key: Yellow = 1 ns trace delay; blue=333 ps, red=100 ps

The basic formula for characteristic impedance is:

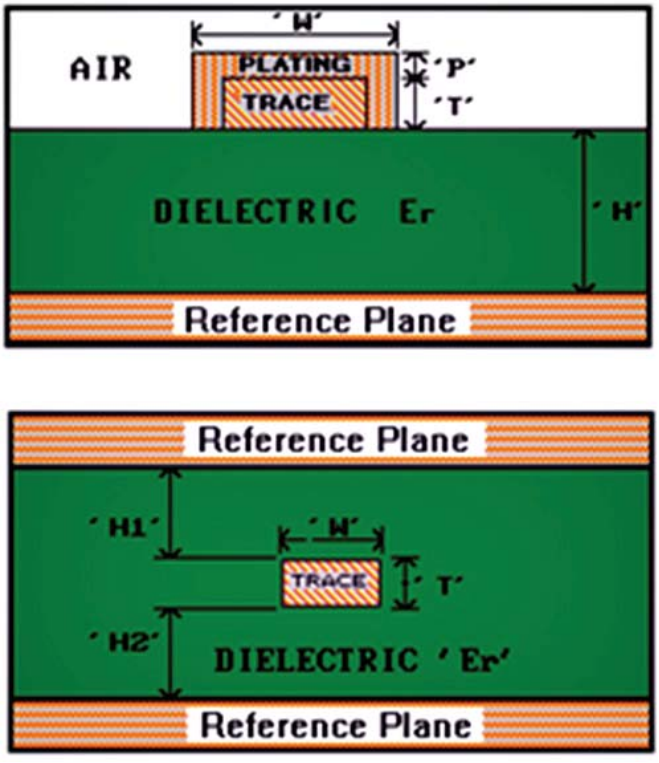
$$Z_o = \sqrt{\frac{L}{C}}$$

Characteristic Impedance

We can see that impedance comprises the capacitive and inductive properties of the trace. So what does this mean to a board designer? You can impact the impedance of your traces largely based on your stack up design. The main things in the stack up that we can use to control the impedance are: dielectric thickness, dielectric constant, and trace width. The copper thickness can also play a part but it isn't one of the primary knobs we use to adjust and control impedance.

With dielectric thickness, we're trying to determine how far away the trace should be placed from its reference layer(s). This is often ground for ideal situations but it could be a power layer as well.

We also need to consider that the trace could be a microstrip (on the outer layer of the board) or a stripline (on an inner layer with references above and below the trace) structure. There are other types of structures such as dual striplines or buried microstrip but I just wanted to provide an example of two of the primary types of structures you'll deal with. In both examples, when you decrease the dielectric thickness, you'll decrease the impedance. Likewise, increasing thickness will increase impedance. Generally, for the same dielectric thickness and trace width, you'll have a higher impedance on a microstrip line than you will for a stripline because of the additional capacitance provided in the stripline structure.



Stripline and Microstrip Structures

The other important piece relative to the dielectric is the dielectric constant. Standard FR4 material in most PCBs will have a relative dielectric constant (commonly seen as ***Er*** or ***Dk*** — these two symbols are interchangeable) on average of about 4.3 but if you choose a dielectric with a much lower ***Er***, it will cause the impedance to increase. Similarly, if you were to increase the ***Er***, it would reduce the impedance. The lever you have to control the ***Er*** is the laminate you choose for the stack up design. If you want to see your options in more exotic materials, check out Isola or Rogers who are just two options of several in the laminate material industry.

The last factor that can play a major part in trace impedance is the trace width. If you increase the trace width, the impedance will go down. If you decrease the width, the impedance will go up.

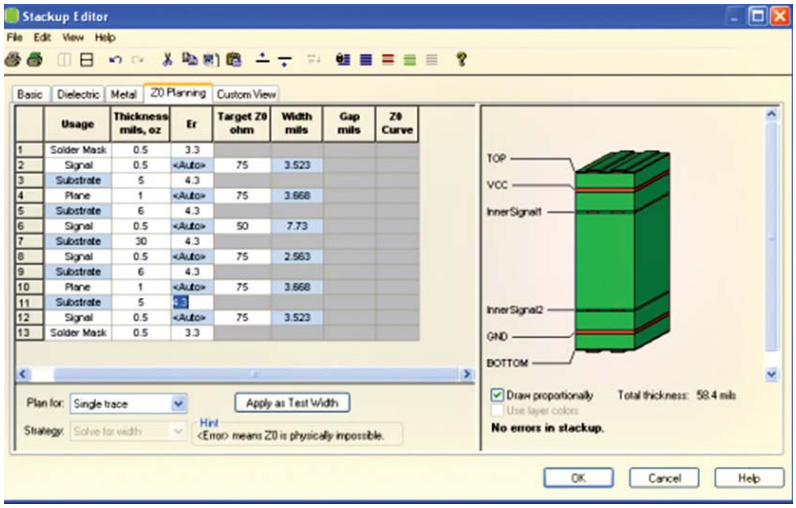
So what makes all these properties behave the way they do? You can trace most of the changes down to how the capacitance is calculated. Looking at the equation for capacitance in a parallel plate, we can see there is dependency on dielectric constant, separation between the plates (***d***), as well as the area (***A***).

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

Capacitance of Parallel Plates

We can see that if the ***Er*** changes, it has a direct relationship on the capacitance. And going back to the characteristic impedance equation, it has an inverse relationship on impedance (e.g. ***Er*** goes up therefore impedance goes down). We can also see that as the separation between the two parallel plates increases, it has an inverse relationship on the capacitance, which means it has a direct relationship with the impedance (e.g. separation goes up therefore capacitance goes down therefore impedance goes up). And lastly, the area changes based on the trace width, so if the trace width goes up, capacitance goes up, which means the impedance goes down.

There are stack up planning tools in HyperLynx that can simplify your life when it comes to impedance planning. It can be as simple as entering a target impedance for a layer given a certain stack up and HyperLynx will tell you the trace width you need. Or you can enter a width and it will give you an impedance on any given layer.



I'll leave you with some final thoughts on impedance control from a practical perspective. For most companies, if you design impedance controlled boards, your manufacturer is going to adjust whatever values you give them to hit the target impedances based on the materials they have on-hand. You may specify 6 mil width for traces and they may do 5.6 mil in production, but the end result that matters is that they are meeting your target impedance.

One trick to give your manufacturer more ability to hit impedance goals is to specify slight differences in trace width for your targeted impedances, especially when it comes to differential impedance. For instance, on Layer 4 of your stack up, you may have a 50 ohm target impedance that results in a 5 mil trace width for single-ended traces, and a 100 ohm differential impedance with 5 mil traces on the same layer. For the single ended traces, just put 5.1 mil into your design and for the differential, make it 4.9 mils. That will allow them to target both impedances for you independent of each other without having to make compromises to either target impedance.

CONCLUSION

This paper is intended to give you some basic fundamentals in signal integrity, not make you an instant expert. If you'd like to learn more about signal integrity and how HyperLynx can help you identify problems such as those discussed in this paper, check out the HyperLynx Signal Integrity Virtual Lab at http://www.mentor.com/pcb/product-eval/hyperlynx-si-virtual-lab. It's a great resource to get up to speed on how to perform simulations for the most common signal integrity issues in your PCB design.

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