POWER | designer

Expert tips, tricks, and techniques for powerful designs

No. 118

Saving Energy via Smart Power Management

— By Michael Drake, Applications Engineer

Power management techniques and methodologies are expanding rapidly. Political, environmental, and consumer-driven pressures are pushing the market toward increasing functionality while decreasing power consumption. Portable applications, in particular, are presently seeing a great deal of expansion. It is a growing market segment that is being fueled by the increase of wireless devices and their expanding feature sets. Cellular telephones, PDAs, MP3 players, digital cameras, and portable gaming platforms are getting smaller, faster, and more capable. In order to maintain acceptable levels of "talk-time" (battery life), a great deal of effort is being put into the design of the power-supply subsystems.

Power conversion and system energy management are two primary areas that affect battery life in portable equipment. Power conversion deals with the efficient transformation of the battery voltage into the required supply rail(s), while system energy management attempts to conserve energy by optimizing the entire system to the real-time needs of the application.

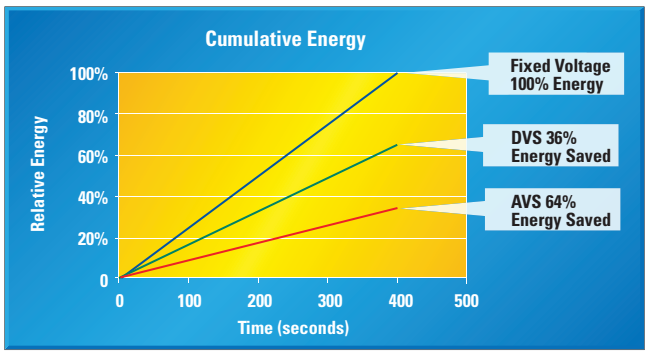

Figure 1. Energy Savings with DVS and AVS

Optimizing Regulation Yields Energy Solutions

The power conversion challenge is to maximize the efficiency of the regulators. The efficiency of a regulator is defined as the output power over the input

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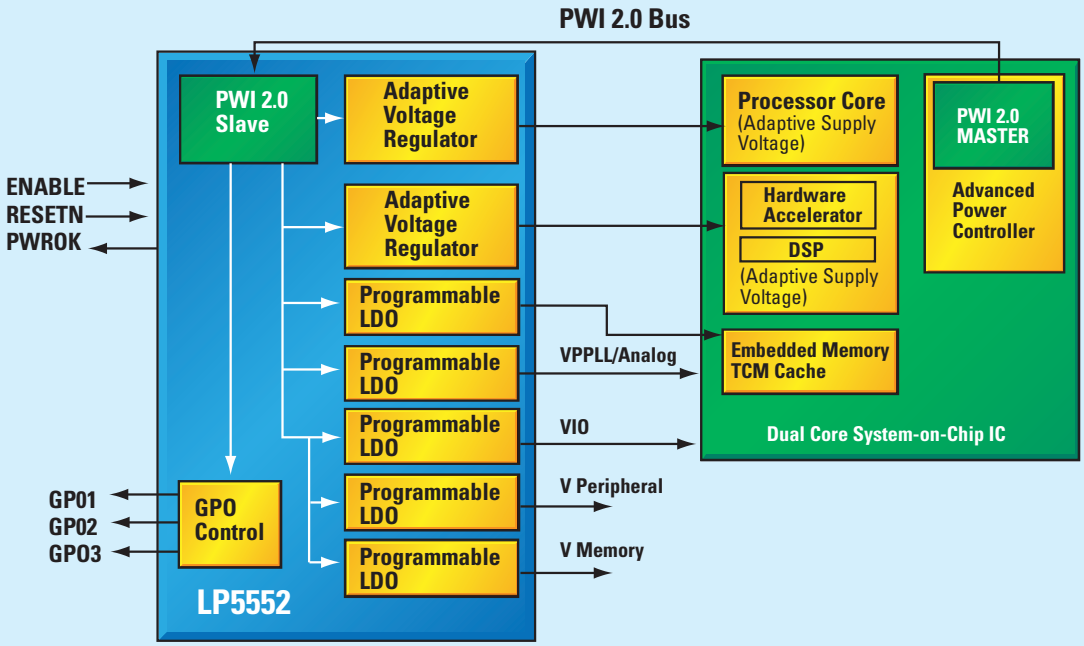
Reduce Energy Consumption with PowerWise® Technology

Digitally-Programmable LP5552 Energy Management Unit Extends Battery Life and Enables New Features



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Product ID	# of Outputs	Output Voltages and Current	V_{IN} Range	Interface	Package
LP5550	4	1 Buck: 0.6V to 1.2V, 300 mA 3 LDOs: 0.6V to 3.3V, up to 250 mA	3V to 5.5V	PWI 1.0	LLP-16
LP5551	8	2 Bucks: 0.6V to 1.2V, 300 mA 4 LDOs: 0.6V to 3.3V, up to 250 mA N-well bias: -0.3 to +1V (to supply) P-well bias: -1V to +0.3V (to GND)	2.7V to 5.5V	PWI 1.0	LLP-36
NEW **LP5552**	7	2 Bucks: 0.6V to 1.235V, 800 mA 5 LDOs: 0.6V to 3.3V, up to 250 mA	2.7V to 4.8V	PWI 2.0	micro SMD-36

Ideal for use in dual core processors, cellular handsets, handheld radios, PDAs, battery-powered devices, and portable instruments

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power and is given as a percentage:

$$\eta = P_{OUT} / P_{IN} = (V_{OUT} * I_{OUT}) / (V_{IN} * I_{IN})$$

Power conversion efficiencies now reach into the 90th percentile and increases are becoming more difficult to realize. As conversion efficiency has reached a plateau, it has become necessary to find new ways to conserve energy at the system level. This gets into the realm of energy management.

The following two equations show the necessity for system energy management. There is the dynamic term involving C, the circuit capacitance, the supply voltage, V_{DD}, and *f*, the clock frequency. The second term is the static term which is dominated by the leakage current of the digital gates. In larger-geometry devices, the dynamic term dominates the power utilization. As the industry moves to ever-smaller devices, the static term is becoming increasingly important.

In a digital system, the power consumed is roughly equal to:

$$P = (C * V_{DD}^2 * f) + (V_{DD} * I_{LEAK})$$

Thus, the energy expended is roughly equal to:

$$E = (C * V_{DD}^2) + ((V_{DD} * I_{LEAK}) * t)$$

Several Techniques Exist for Design Improvements

Almost all large digital systems will deploy one or more clock-gating strategies to avoid unnecessary toggling of the clock, and many systems will power-down unused sections of the design when appropriate. Processing engines also make use of idle and sleep modes to save energy. This is a conventional energy management technique whereby the processor wakes up periodically, or when required, performs its pending tasks, and then returns to a low-power state. These techniques can be effective, but come at a cost. Any time the circuitry is needed, there is some delay while it is powered up and/or synchronized. These methods conserve energy only when there is nothing to do (i.e., when the processor is in the sleep state).

Newer techniques have involved scaling the frequency and voltage of the processing engine to reduce energy expenditure. Energy is the key metric for increasing ON-time in dealing with battery-powered systems. Dropping the frequency alone will reduce the average power consumption, but it will not reduce the total energy used to complete a specific computational task. The voltage in the system must be reduced to realize energy savings. Dynamic Voltage Scaling (DVS) and Adaptive Voltage Scaling (AVS) both can achieve a reduction in voltage, refer to Energy Savings with DVS and AVS in ***Figure 1***.

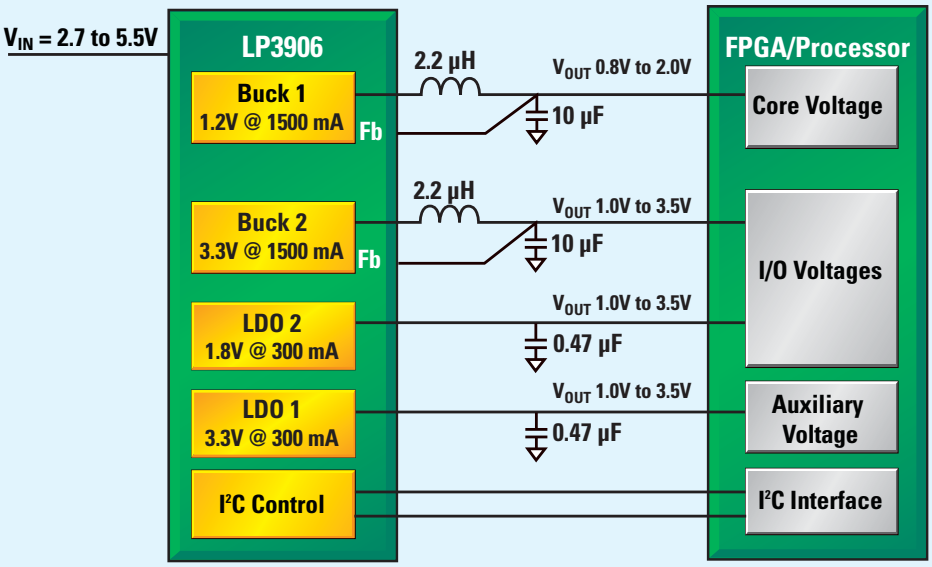
DVS adjusts the voltage and frequency in pre-characterized pairings. National Semiconductor offers Power Management ICs (PMICs) such as the LP3906 and LP3907 devices which support DVS mode as well as devices which support both AVS and DVS modes such as the LP5550, LP5551, and LP5552. DVS provides power and energy savings, with some additional margin in the voltage to accommodate all potential systems over process and temperature variations. This extra overhead to accommodate the worst case results in wasted energy in non-ideal systems. If it was possible to close the power-supply loop at the system level, the control loop could adaptively scale the voltage to the minimum workable voltage and conserve the most energy. PowerWise® technology accomplishes that.

The PowerWise Interface (PWI®) Enables Smart Energy Management

The PowerWise specification is a system-level approach to energy management that enables Adaptive Voltage Scaling (AVS) and state control for battery-powered devices. The PowerWise concept incorporates closed-loop AVS with a high-speed, serial-power-management bus to allow a processing engine to use the minimum voltage at any operating frequency, at any given time in the system, to minimize dynamic energy dissipation.

Easy-to-Use Power Management Units for Digital Subsystems

96% Efficient LP3906 Provides Flexibility with Digital Programmability



LP3906 Features

- Two programmable buck regulators to support core and other high-current rails
- Two programmable LDOs to support internal processor functions and peripherals
- I²C for independent control of LP3906 and peripherals

Ideal for powering application processors, FPGAs, and DSPs where size and efficiency are important

Product ID	Digitally Programmable	Efficiency	Regulator Output Current	LDO Output Current	Packaging	Solution Size
LP3906	I²C	Up to 96%	1.5 A	300 mA	LLP-24	20 mm x 20 mm
LP3905	N/A	Up to 90%	600 mA	150 mA (low noise)	LLP-14	15 mm x 10 mm

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PowerWise technology also incorporates the ability to bias the well voltages of a processing engine. As V_{DD} is reduced to minimize dynamic losses, the threshold voltage of the transistors must also be reduced to maintain high drive levels. This increases the leakage current and static-power losses. The leakage current can be reduced by back-biasing the well. Alternatively, by forward-biasing it, higher drive levels can be achieved for the same V_{DD}. The PowerWise loop and well-biasing schemes may be used in conjunction with multi-V_T designs.

The standard system configuration to enable PowerWise closed-loop AVS is comprised of an Advanced Power Controller (APC) residing in the processing engine, a PMIC containing a PWI slave, and the 2-wire PWI serial bus connecting the two components. The PMIC supplies various voltages to the processor. The voltage levels provided by the PMIC can be adjusted by sending commands from the PWI master within the APC to the PWI slave.

The APC's task is to accept commands from the host processor, provide a CPU-independent voltage-control mechanism, and track the logic operating speed in real time. The APC is always active and continuously monitors the system over all parameters. System temperature, load, transient, and process variation, amongst others, are all accounted for. As the APC is informed of a pending frequency change, it determines the minimum voltage possible for stable system operation at the new frequency. This occurs within the closed loop to servo the voltage to the appropriate level by using voltage-adjustment commands issued by the APC to the PWI slave via the PWI interface.

Options for Meeting Power Challenges

The PowerWise AVS technology is available with two APC versions. APC1 is for simple single-voltage domain designs and APC2 is suited for more complex multi-domain systems. APC1 uses the point-to-point PWI 1.0 interface while APC2 utilizes the PWI 2.0 bus interface between the master(s) and slave(s).

National offers two Energy Management Units for APC1: the LP5550 device, which includes one AVS DC-DC switcher and three LDOs, and the LP5551 device which adds another DVS-style DC-DC switcher, an additional LDO, and bias regulators for N- and P-well connections in threshold-scaling applications.

The LP5552 Energy Management Unit is compatible with the APC2/PWI 2.0 IP package. The LP5552 device contains two high-performance switching regulators for AVS or DVS applications and five LDOs. All seven regulators are contained in the tiny 36-bump micro SMD package. Each regulator can be independently turned on and off as well as programmed to a desired voltage.

Higher Switching Frequency Enables Reduced Power and Circuit Size

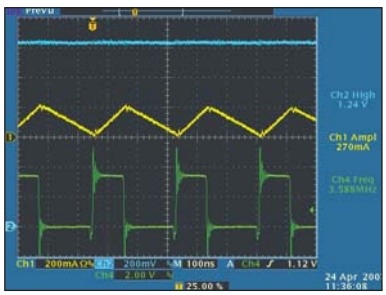
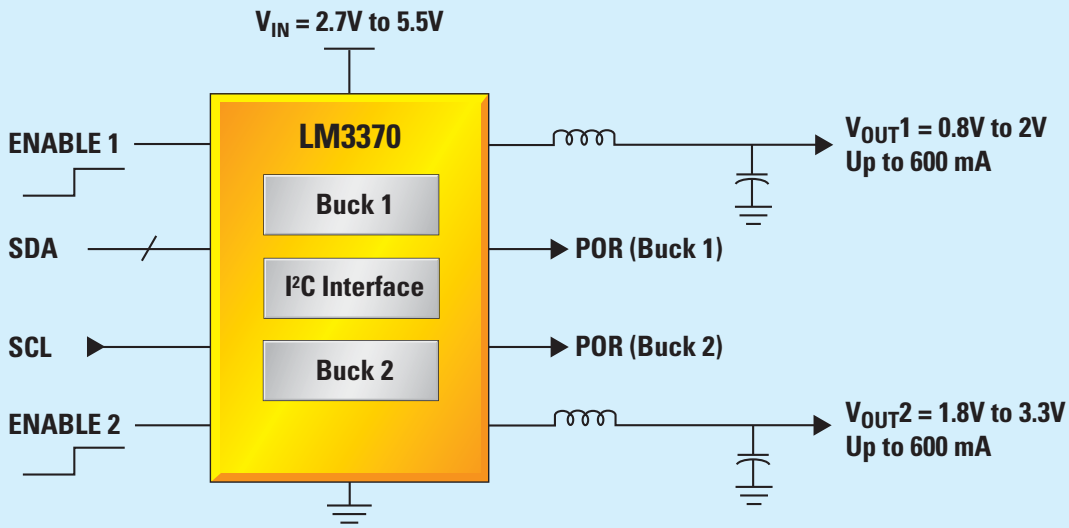


Figure 2. Switcher Output at V_{IN} = 3.6V, V_{OUT} = 1.235V, I_{LOAD} = 400 mA Load

The switching regulators in the LP5552 device operate at a switching frequency of 3.6 MHz as seen in ***Figure 2***. The increased switching frequency allows the use of smaller-valued components for the output filter. Typical values are a 1 µH inductor and a 10 µF ceramic capacitor. These smaller values allow the system designer to select smaller footprint parts with low vertical heights, while maintaining outstanding transient performance.

Enhance Digital Processor Power Management with Dynamic Voltage Scaling (DVS)

LM3370 Dual Buck Regulator Provides Highest Efficiency for FPGAs and Multimedia Processors

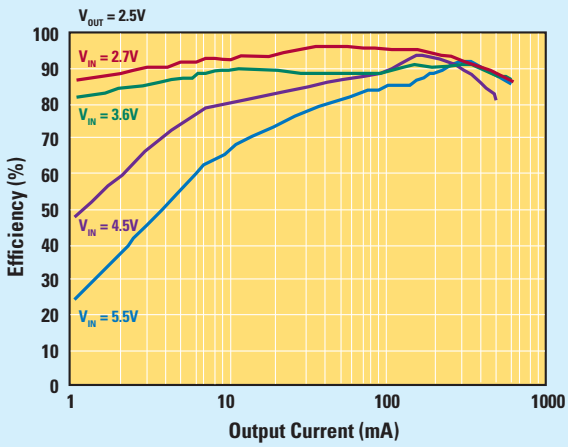


LM3370 Features

- Automatic PFM-PWM mode switching provides high efficiency at all loads
- I²C-compatible interface scales power to match processor clock frequency
- Lowest Iq (<20 µA) extends battery life
- 2 MHz operation enables smaller external components and minimizes footprint
- Power-on-reset prevents fault condition in processors
- Spread spectrum reduces noise (ideal for RF systems)

Ideal for low-power FPGAs, CPLDs, and application processors

High Efficiency Across All Loads



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Transient performance of the switchers can be seen in ***Figure 3***. The entire power system can be realized in a sub-0.85 mm height allowing extremely thin form factors in the product design.

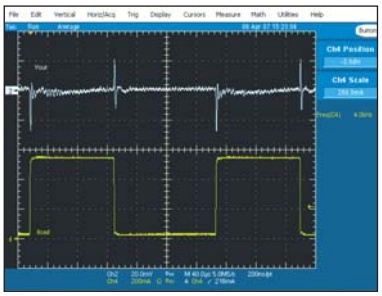

Figure 3. 50 mA to 560 mA to 50 mA Load Transient at 300 mA/µS

Key Features

The switchers are capable of operating at a maximum DC current of 800 mA with peak efficiencies of 88%. The switchers are digitally programmable from 0.6V to 1.235V in steps of 5 mV. ***Figures 4 and 5*** show the settling time of the output being programmed to minimum (0.6V) and to maximum (1.235V). Each switcher also has an associated memory-retention LDO that can be programmed to track the switcher voltage for voltage-scaling applications, or can be used as an independent 50 mA LDO. These two memory-retention regulators can be programmed between 0.6V and 1.35V, in 50 mV steps.

The three remaining LDOs offer designers flexibility in powering other regions of the design. There are two 300 mA-output LDOs, one of which sets the I/O signaling environment for the LP5552 device, and presumably the system.

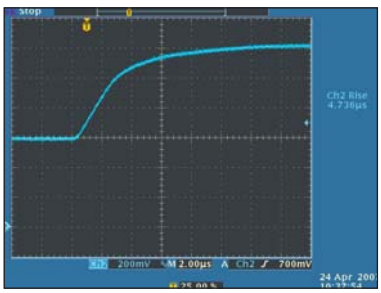

Figure 4. V_{OUT} Min to Max Settling Time with No Load

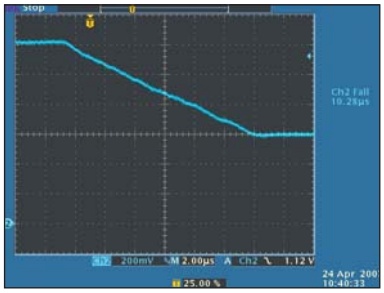

Figure 5. V_{OUT} Max to Min Settling Time with No Load

The third LDO, intended to power PLLs and/or analog functions, is capable of 100 mA of continuous output current. All of these LDOs are digitally programmable as well.

The LP5552 device has a number of additional signals to allow seamless integration of the LP5552 into the target system. ENABLE and RESETN can be used in the system to handle power sequencing, register space resets, and global power on/off. The PWROK signal is an indicator that can be used for power sequencing or power-on-reset generation. The LP5552 device also includes three GPOs that can be freely used as extra digital drivers in the system. The system designer can program them to be either an open-drain output or a push-pull output referenced to the LP5552 I/O voltage.

The LP5552 device can greatly simplify system design, minimize cost, and save PCB space. It is a very dense package that can fill most needs for a portable power system. Coupled with a PWI 2.0 master, operating in closed-loop AVS, it can realize the greatest energy savings in portable equipment. It can also be used in an open-loop DVS application, and the PWI traffic may be bit-banged from GPIOs on a processing engine without an APC. The PowerWise Interface specification can be freely downloaded and implemented at www.pwistandard.org. Information about National's PowerWise technology offerings, as well as all other power management solutions, can be found at power.national.com. ■

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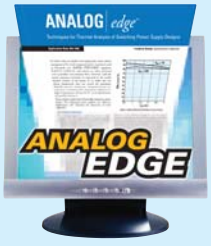

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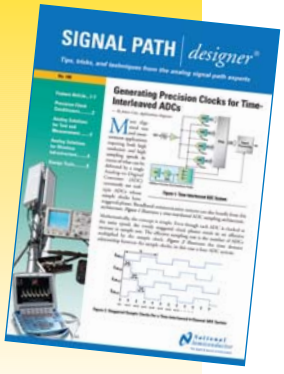

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